UART Theory of Operation

# Purpose

This document outlines how the Field Programmable Gate Array (FPGA) Universal Asynchronous Receiver/Transmitter ([UART](http://en.wikipedia.org/wiki/Universal_asynchronous_receiver/transmitter#Character_framing)) based implementation is intended to work.

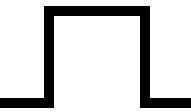
# Transmitter Theory

Baud Rate = Bits/s

Clock Rate = Loop Rate

Generation Rate (ticks)= Clock Rate/Baud Rate

* Example – 100MHz/115200 = 868.05 ticks per pulse



Start Bit = Logic low, represent the start of a Character Frame

Character Length = Typically 8 bits (can be other values)

Stop Bits = Number of high bits after the data bits and parity(if present)

[Parity](http://en.wikipedia.org/wiki/Parity_bit) = Used to detect errors (even or odd parity)

Character Spacing = Number of Characters/time duration post stop bit/s before the next character can be processed.

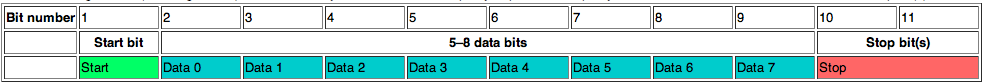


Figure : Example Character Frame

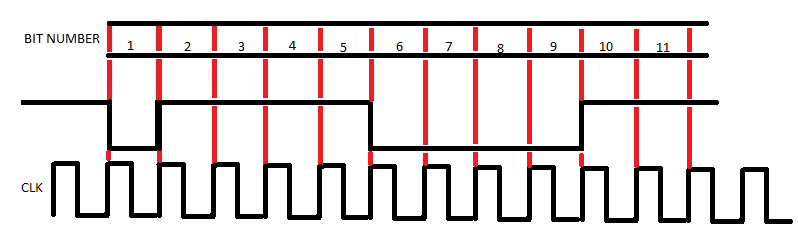


Figure : Example Character Frame with CLK signal

In Figure 2 the data value of the character frame is 0x0F.

Bit 1 = Start Bit

Bits 2-5 = Data value of F

Bits 6-9 = Data value of 0

Bits 10-11= 2 Stop Bits

## Execution

\*Data is changed on the rising edge of the CLK.

1. The Tx Line will be sent a 0, this initiates a start to be sent to the receiver.

2. Generate N number of bits correspond to the Character Length.

3. Optional: A Parity bit may be sent (even or odd).

4. Stop Bit/s will be generated (typically 1, 1.5, or 2).

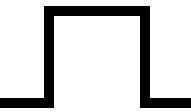
# Receiver Theory

Baud Rate = Bits/s

Clock Rate = Loop Rate

Generation Rate (ticks)= Clock Rate/Baud Rate

* Example – 100MHz/115200 = 868.05 ticks per pulse



Start Bit = Logic low, represent the start of a Character Frame

Character Length = Typically 8 bits (can be other values)

Stop Bits = Number of high bits after the data bits and parity(if present)

[Parity](http://en.wikipedia.org/wiki/Parity_bit) = Used to detect errors (even or odd parity)

## Execution

1. The Rx Line will be receive a 0

2. Find RxCenter

* This is calculated by ((Clock Rate/Baud Rate)/2)
* Example ((100MHz/115200)/2) = 434.02 ticks
* Shift the acquisition by 434.02 ticks, this ensures the data will be sampled at a safe time (avoid metastable events).

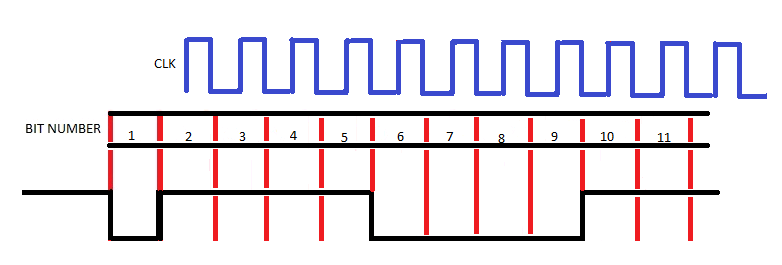


Figure : Example Receiver with CLK

\* Blue signal represents when the data is acquired after the shift.

3. Acquire N number of bits correspond to the Read Character Length.

4. Optional: A Parity bit may be acquired (even or odd), if an entire bit frame passes without the correct parity bit, throw a parity error

5. Stop Bit/s will be acquired (typically 1, 1.5, or 2). If proper number of stop bits isn’t acquired, throw a frame error.

6. Optional: Character spacing wait to acquire next start bit by N number of bits.

# Appendix A:

Clock Frequency is 100MHz at 16

Formulas:

UBRR = (CLK Freq/(16 \* BAUD)) – 1

BAUD = CLK Freq / (16 \* (UBRR+1))

Error% = ((Baud\_close/Baud\_want) - 1) \* 100%

|  |  |
| --- | --- |
| Requested Baud | % Difference |
| 110 | 0.0003 |
| 300 | 0.0016 |
| 600 | -0.0003 |
| 1200 | 0.006 |
| 2400 | 0.006 |
| 4800 | 0.006 |
| 9600 | 0.006 |
| 14400 | 0.006 |
| 19200 | -0.15 |
| 28800 | 0.006 |
| 38400 | -0.15 |
| 56000 | -0.35 |
| 57600 | -0.45 |
| 115200 | 0.47 |
| 128000 | -0.35 |
| 153600 | -0.76 |
| 230400 | 0.47 |
| 256000 | 1.73 |
| 460800 | -3.12 |
| 921600 | -3.12 |